



EXPEDITED PROCEDURES
RESPONSE AFTER FINAL

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

Myung-Koo HUR, *et al.*

Serial No.: 09/196,185

Confirmation No.: 8847

Filed: November 20, 1998

Docket No.: 6192.0052.AA

Group Art Unit: 2871

Examiner: QI, Zhi Qiang

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For: **WIRES FOR LIQUID CRYSTAL DISPLAYS, LIQUID CRYSTAL DISPLAYS
HAVING THE SAME, AND MANUFACTURING METHODS THEREOF**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR RECONSIDERATION UNDER 37 C.F.R. § 1.116

Sir:

In response to the Final Office Action mailed August 9, 2004 (Paper No. 20040728) (“Office Action”), Applicants respectfully request reconsideration of the application in view of the following Remarks.

Applicants believe that no extensions of time are required at this time. If extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned for under 37 C.F.R. § 1.136(a). Applicants believe that no further fees for net addition of claims are required at this time. Any fees required for further extensions of time and any fees for the net addition of claims are hereby authorized to be charged to our Deposit Account No. 23-1951.

14. (Previously Presented) A thin film transistor (TFT) panel, comprising:
- an insulating substrate;
- a gate wire formed on the substrate and comprising a gate line, a gate electrode and a gate pad;
- a gate insulating layer covering the gate wire;
- a semiconductor layer formed on said gate insulating layer;
- a data wire formed on the semiconductor layer comprising a data line, a source electrode and a drain electrode;
- a passivation layer formed on the data wire and the gate wire and having a first contact hole extended to the gate pad and a second contact hole extended to the drain electrode; and
- a transparent conductive layer formed on the passivation layer and connected to the gate pad through the first contact hole and the data wire through the second contact hole,
- wherein at least one of the gate wire and the data wire comprises a main layer and a supplemental layer, and
- the supplemental layer is substantially inert to an etchant used for etching the transparent layer for preventing the gate pad or the data wire from being eroded by the etchant.

21. (Previously Presented) The TFT panel of claim 14, wherein the transparent conductive layer is formed of indium tin oxide (ITO).

22. (Previously Presented) The TFT panel of claim 21, wherein the transparent conductive layer comprises:

a gate ITO layer connected to the gate pad through the first contact hole; and
a pixel electrode connected to the drain electrode through the second contact hole.

23. (Previously Presented) The TFT panel of claim 14, wherein the main layer comprises metal or a metal alloy.

24. (Previously Presented) The TFT panel of claim 23, wherein the supplementary layer comprises metal nitride or metal alloy nitride.

25. (Previously Presented) The TFT panel of claim 24, wherein the supplementary layer further comprises one selected a group consisting of tungsten, chromium, zirconium and nickel.

26. (Previously Presented) A thin film transistor (TFT) panel, comprising:
an insulating substrate;
a gate wire formed on the substrate and comprising a gate line, a gate electrode and a gate pad;
a gate insulating layer covering the gate wire;
a semiconductor layer formed on said gate insulating layer;
a data wire formed on the semiconductor layer comprising a data line, a source electrode and a drain electrode;

a passivation layer formed on the data wire and the gate wire and having a first contact hole extended to the gate pad and a second contact hole extended to the drain electrode; and a transparent conductive layer formed on the passivation layer and connected to the gate pad through the first contact hole and the data wire through the second contact hole, wherein at least one of the gate wire and the data wire comprises a main layer and a supplemental layer, and the main layer comprises metal or a metal alloy, and the supplementary layer comprises metal nitride or metal alloy nitride.